REMARKS

Applicants acknowledge the withdrawal of claims 31-32 and 34-37 from consideration.

The Drawings have been objected to because of the lack of description of reference number 12. This informality has been corrected with the above amendment to the text, and no change to the Drawings is deemed necessary.

Claims 1, 6-11, 14-20, 22-24, 26, and 28-30 have been rejected under 35 USC 102(b) as being anticipated by Koizumi '892.

Of the claims under rejection, claims 1, 11, and 20 are independent. Although the various claims are directed to, respectively, a chip, an apparatus having a chip, and a wafer (from which chips can subsequently be diced), at least one feature is common to all of the independent claims: the chip includes a **portion of a groove** which defines an edge of the chip. A light-transmissive planar layer extends **over** this portion of the groove.

An embodiment of this claimed feature is shown in the specification as filed at Figure 3 for a chip which has not yet been diced from a wafer. Each chip 10 defines an edge having a portion of a groove 70. Although the side of the groove 70 slants downward from the main (top) surface of a chip 10, because the planar layer 72 extends over the portion of the groove 70, the overall top surface of the resulting chip 10, such as shown as the material to the right of cut line 71, is made planar even over the groove 70.

In the rejection, as an instance in the prior art of "the planar layer extending over the groove portion," there is cited column 2, lines 57-58 of Koizumi. The cited portion, it must be noted, is part of a larger discussion of a process described in the reference. The series of steps shown in Figure 11, as noted by the Examiner, generally correspond to the claimed structures and methods. However, close examination of the *entire* method and its resulting product show key differences between the reference and the claims, as noted at Column 2, lines 56-67 of Koizumi (emphasis added):

> In order to eliminate steps on the device surface, the entire surface of the device is coated with a transparent resist [FIG. 11C]. Then, coating and patterning for red (96), blue (98), and green (99) color filters are sequentially repeated, thus forming color filters [FIG. 11D]. Furthermore, in order to protect the respective filters, a passivation layer is formed on the entire surfaces of the respective color filters [FIG. 11E]. **Finally, a transparent resin in each scribe region is removed** [FIG. 11F]. **Thereafter,** respective solid-state image pickup **chips are cut along the scribe regions** using, e.g., a dicing cutter.

It is clear from this description that, prior to dicing the wafer into chips, the scribe line/groove portion of the wafer, such as shown as C, is indeed planarized with transparent resist; however, as is perfectly clear by the above passage and Figure 11F of Koizumi, immediately before the dicing step the transparent resist, or the light-transmissive layer, is ***completely removed from the groove C.*** Therefore, **no part** of the light-transmissive layer in Koizumi can be said to *extend into the area* corresponding to groove C in either the wafer (immediately pre-dicing) or the finished chip, as recited in every indepen dent claim.

Independent **claims 1 and 11** both positively recite that the light-transmissive planar layer extends over the groove portion at the edge of the chip, a structure that would clearly be impossible to achieve with the wafer as shown in Figure 11F of Koizumi, where the planarizing layer is clearly *removed* from the groove before the wafer is diced into chips. Independent **claim 20**, directed to a wafer, has been amended to recite positively that the wafer as claimed is suitable "for immediate dicing" into at least one chip, which means that the light-transmissive layer in the groove *remains in the groove* up to the point of dicing.

The practical advantage provided by this chip and wafer configuration is given at pages 2 and 8 of the specification as filed (emphases added):

> One problem concerns the inadvertent ripping or other damage to the cured filter layers when the wafer is diced into individual chips: **the relatively thin translucent filter layer**, particularly at the photosensors toward either end of the chip, **can be torn by th action of a saw blade.**

* * *

[With the present invention, w]hen a wafer is diced, such as along a groove 70, [because of] the fact that each filter layer 74 is disposed over and supported by clear [planar] layer 72, which itself takes up most of the void formed by the groove 70, **the filter layer 74 exhibits very little damage or tearing**, especially in the portions thereof around any photosites 14.

In short, the planarizing layer *allowed to remain within the groove* prevents or lessens damage to a filter layer during a dicing process. This practical advantage is not available in Koizumi, where the planarizing layer is explicitly *removed* from the groove before dicing.

In the Final Office Action, the assertion is made that the fact Koizumi removes the planarization layer before dicing has "nothing to do with the rejection since the examiner rejected the claim because the examiner rejected the claim[s] using the Figs. 11C and 11D [of Koizumi], which show the chip before removing the light-transmissive layer." In response, Applicants point out that the *precise wording* of each independent claim distinguishes the claimed invention from the disclosure in Figs. 11C and 11D of Koizumi: the independent claims at issue relate to either a chip, a chip as part of a larger apparatus, or to a wafer "suitable for immediate dicing" into a chip. The disclosed structures in Figs. 11C and 11D do not relate to a chip nor to a wafer suitable for immediate dicing. In the cited figures, we are looking at, purely, a *wafer*— **not a chip**, because a chip is a wafer which has been diced, and the wafer in Figs. 11C and 11D *has not been diced.* Therefore, the cited Figures do not teach the invention of claims 1 or 11, which relate unambiguously to a **chip.** Nor are the disclosed structures in Figs. 11C and 11D of a wafer "suitable for immediate dicing" into a chip, as in independent claim 20: by the disclosure of Koizumi itself, the structure of Figs. 11C and 11D must go through *at least* the steps of Figs. 11E-F (which describe the *removal* of the planarization layer) before any dicing is contemplated. Therefore, the specific cited art, Figs 11C and 11D of Koizumi, does not teach the invention of claim 20: a wafer "suitable for immediate dicing."

Claims 2, 12, and 21 are rejected under 35 USC 103 over Koizumi. Claims 3, 13, and 25 are rejected under 35 USC 103 over Koizumi, as applied to their respective independent claims, and further in view of Jedlicka, which discloses the use of acrylic for a filter layer. These claims are deemed allowable as being dependent upon their respective independent claims, the patentability has been argued above.

It is respectfully submitted that the present set of claims are patentably distinct over the cited reference. In the event the Examiner considers personal contact advantageous to the disposition of this case, he is hereby requested to call the undersigned attorney at (585) 423-3811, Rochester, NY.

Respectfully submitted,

Robert Hutter
Attorney for Applicant(s)
Registration No. 32,418
Telephone (585) 423-3811

June 16, 2003
RH/fsl
Xerox Corporation
Xerox Square 20A
Rochester, New York 14644

VERSION WITH MARKINGS TO SHOW CHANGES MADE:

IN THE SPECIFICATION:

Figure 1 is a plan view of a single photosensitive chip, generally indicated as 10, of a design found, for example, in a full-color photosensor scanner or digital camera. A typical design of a full-page-width scanner will include a plurality of chips 10, each chip being approximately one-half to one inch in length, the chips being butted end-to-end to form an effective collinear array of photosensors, which extends across a page image being scanned. Each chip 10 is a silicon-based integrated circuit chip having defined in a main surface thereof three independently-functioning linear arrays of photosensors, each photosensor being here indicated as 14. A number of contact pads 12 are used for external circuitry to interact with circuitry (not shown) inside the chip 10, such as to provide instructions to the chip 10 or receive video signals from the chip 10. The photosensors are disposed in three parallel rows which extend across a main dimension of the chip 10, these individual rows being shown as 16A, 16B, and 16C. Each individual row of photosensors on chip 10 can be made sensitive to a particular color, by applying to the particular row a spectrally translucent filter layer which covers only the photosensors in a particular row. In a preferred embodiment of the present invention, the three rows of photosensors are each filtered with a different primary color, such as red, green, and blue. Generally, each individual photosensor 14 is adapted to output a charge or voltage signal indicative to the intensity of light of a certain type impinging thereon; various structures, such as transfer circuits, or charge-coupled devices, are known in the art for processing signal output by the various photosensors corresponding to photosites 14.